APPLICATION NO 10/609185

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CLMPTO

1. A semiconductor device comprising:

   a layer of semiconductor material;

   a plurality of regions of first and second opposite conductivity-types disposed in the layer of semi-conductor material;

   one region of the plurality comprising an anode-emitter;

   another region of the plurality of regions comprising a cathode-emitter;

   the cathode-emitter of conductivity type opposite to that of the anode-emitter;

   at least two regions of the plurality of regions disposed between the anode-emitter and the cathode-emitter;

   the anode-emitter defining a junction where it meets one of the at least two regions;

   a first electrode disposed over at least one of the regions between the anode and the cathode emitters; and

   epitaxial material on the cathode and/or anode-emitter regions of the layer of semiconductor material;

   the epitaxial material offset laterally from and clear of the junction of the anode and/or cathode emitter region(s) at the surface of the layer of semiconductor material.

2. The device of claim 1, further comprising silicide on at least a portion of the epitaxial material.

3. The device of claim 2, the first electrode comprising polysilicon and silicide on at least a portion of the polysilicon as a gate electrode.

4. The device of claim 2, in which

the epitaxial material comprises a peripheral edge where it meets the surface of the layer of semiconductor material; and

the layer of semiconductor material comprises a region between the peripheral edge of the epitaxial material and the first electrode that is free of silicide.

5. The device of claim 4,

the anode-emitter, the cathode-emitter , and the at least two different regions of the alternating regions therebetween defining a thyristor;

the two different regions between the anode and the cathode-emitters to establish first and second base regions respectively of the thyristor; and

the first electrode disposed over a substantial width of the second base region and over a portion of the cathode-emitter neighboring the second base;

the surface region free of silicide between the peripheral edge of the epitaxial material of the anode-emitter and a peripheral edge of the first electrode, extending laterally over a portion of the anode-emitter region, the full width of the first base region of the thyristor and a portion of the width of the second base region.

6. The device of claim 2, further comprising:

a conductor to propagate a reference voltage;

the conductor electrically coupled to the silicide of at least one of the anode and the cathode emitters.

7. The device of claim 6, in which:

the layer of semiconductor material further comprises source, drain and channel regions to define at least in part an access transistor;

one of the source and drain region of the access transistor in common with one of the cathode-emitter and the anode-emitter; and

the device further comprises:

a gate electrode over the channel region of the access transistor, the gate operable under voltage bias to apply an electric field to the channel region; and

epitaxial material on the other of the source and drain region;

silicide on the epitaxial material over the other of the source and the drain region; and

a bitline in electrical contact with the silicide of the other of the source and drain region.

8. The device of claim 7, further comprising:

first and second sidewall spacers against respective first and second opposite sidewalls of the first electrode;

the first sidewall spacer over the cathode-emitter and comprising a first lateral width that extends outward from the electrode; and

the second sidewall spacer comprising a lateral width that extends outward from the electrode by a distance substantially greater than the first lateral width.

9. The device of claim 8, further comprising:

epitaxial material on the shared emitter-source and drain region;

the epitaxial material on the emitter comprising a peripheral edge that is laterally offset from the first electrode by a magnitude related to the first lateral width of the first sidewall spacer; and

the epitaxial material of the anode-emitter laterally offset from the first electrode by a magnitude at least as great as the lateral width of the second sidewall spacer.

10. A memory device comprising:

a thyristor formed in a layer of semiconductor material, the thyristor comprising:

an anode-emitter;

a cathode-emitter; and

first and second base regions of different polarities between the anode-emitter and the cathode-emitter ;

a first electrode over at least a portion of and capacitively coupled to the first base region;

the second base region formed in a position of the layer of semiconductor material that is offset laterally and outwardly from an edge of the first electrode; and

a raised provision of semiconductor material on the layer of semiconductor material as a raised portion of at least one of the anode-emitter and cathode-emitter ;

the raised portion of the anode-emitter comprising sidewalls that define at least in part an outline at the surface of the layer of semiconductor material and spaced laterally from the second base region.

11. The device of claim 10, further comprising:

an access transistor to access the thyristor;

the access transistor comprising source, drain and body regions within the layer of semiconductor material, the body region in contiguous relationship between the source and drain regions; and

raised source and drain provisions on the layer of semiconductor material and over the respective source and drain regions.

12. The device of claim 11, one of the source and drain regions of the access transistor in common with one of the cathode-emitter and anode-emitter of the thyristor within the layer of semiconductor material.

13. The device of claim 11, in which the raised provisions for the anode-emitter, source and drain regions comprise epitaxial material.

14. The device of claim 13, the layer of semiconductor material comprising a layer of silicon over an insulator.

15. The device of claim 14, in which the thickness of the layer of silicon over the insulator is less than 50 nm.

16. The device of claim 11, further comprising silicide on at least one of the raised provisions of the anode-emitter, the source and the drain regions.

17. The device of claim 16, in which each of the thyristor electrode and a gate electrode of the access transistor comprise:

polysilicon in insulated relationship over the layer of semiconductor material; and

silicide on at least a portion of the polysilicon.

18. The device of claim 10, further comprising silicide-blocking material over the layer of semiconductor material and between the raised provision and the first electrode.

CLAIMS 19-57 (CANCELLED)